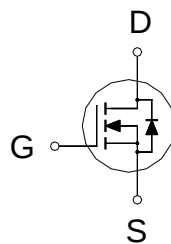


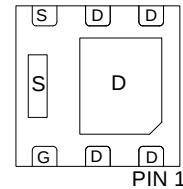
N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV _{DSS}	30V
R _{DS(on)} (MAX.)	11.5mΩ
I _D	9A



Bottom View



UIS, R_g 100% Tested

Pb-Free Lead Plating & Halogen Free



ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V _{GS}	±20	V
Continuous Drain Current	T _A = 25 °C	I _D	9	A
	T _A = 70 °C		5.9	
Pulsed Drain Current ¹		I _{DM}	36	
Avalanche Current		I _{AS}	10	mJ
Avalanche Energy	L = 0.1mH, I _D =10A, R _G =25Ω	E _{AS}	5	
Repetitive Avalanche Energy ²	L = 0.05mH	E _{AR}	2.5	
Power Dissipation	T _A = 25 °C	P _D	2.08	W
	T _A = 70 °C		1.33	
Operating Junction & Storage Temperature Range		T _j , T _{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	R _{θJC}		12	°C / W
Junction-to-Ambient ³	R _{θJA}		60	

¹Pulse width limited by maximum junction temperature.

²Duty cycle ≤ 1%

³60°C / W when mounted on a 1 in² pad of 2 oz copper.

ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	30			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	1	1.7	3	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0V, V_{GS} = \pm 20V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 24V, V_{GS} = 0V$			1	μA
		$V_{DS} = 20V, V_{GS} = 0V, T_J = 125^\circ C$			25	
On-State Drain Current ¹	$I_{D(ON)}$	$V_{DS} = 10V, V_{GS} = 10V$	9			A
Drain-Source On-State Resistance ¹	$R_{DS(ON)}$	$V_{GS} = 10V, I_D = 9A$		9.7	11.5	m Ω
		$V_{GS} = 4.5V, I_D = 6A$		13	16	
Forward Transconductance ¹	g_{fs}	$V_{DS} = 5V, I_D = 9A$		15		S
DYNAMIC						
Input Capacitance	C_{iss}	$V_{GS} = 0V, V_{DS} = 15V, f = 1MHz$		1050		pF
Output Capacitance	C_{oss}			141		
Reverse Transfer Capacitance	C_{rss}			87		
Gate Resistance	R_g	$V_{GS} = 15mV, V_{DS} = 0V, f = 1MHz$		2.3		Ω
Total Gate Charge ^{1,2}	$Q_g(V_{GS}=10V)$	$V_{DS} = 15V, V_{GS} = 10V,$ $I_D = 9A$		17.6		nC
	$Q_g(V_{GS}=4.5V)$			9.0		
Gate-Source Charge ^{1,2}	Q_{gs}			2.6		
Gate-Drain Charge ^{1,2}	Q_{gd}			4.0		
Turn-On Delay Time ^{1,2}	$t_{d(on)}$	$V_{DS} = 15V,$ $I_D = 1A, V_{GS} = 10V, R_{GS} = 6\Omega$		8		nS
Rise Time ^{1,2}	t_r			8		
Turn-Off Delay Time ^{1,2}	$t_{d(off)}$			15		
Fall Time ^{1,2}	t_f			10		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T _c = 25 °C)						
Continuous Current	I_S				9	A
Pulsed Current ³	I_{SM}				36	
Forward Voltage ¹	V_{SD}	$I_F = I_S, V_{GS} = 0V$			1.2	V
Reverse Recovery Time	t_{rr}	$I_F = I_S, di_F/dt = 100A / \mu S$		18		nS
Reverse Recovery Charge	Q_{rr}			10		nC

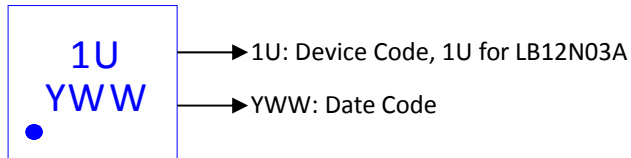
¹Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

²Independent of operating temperature.

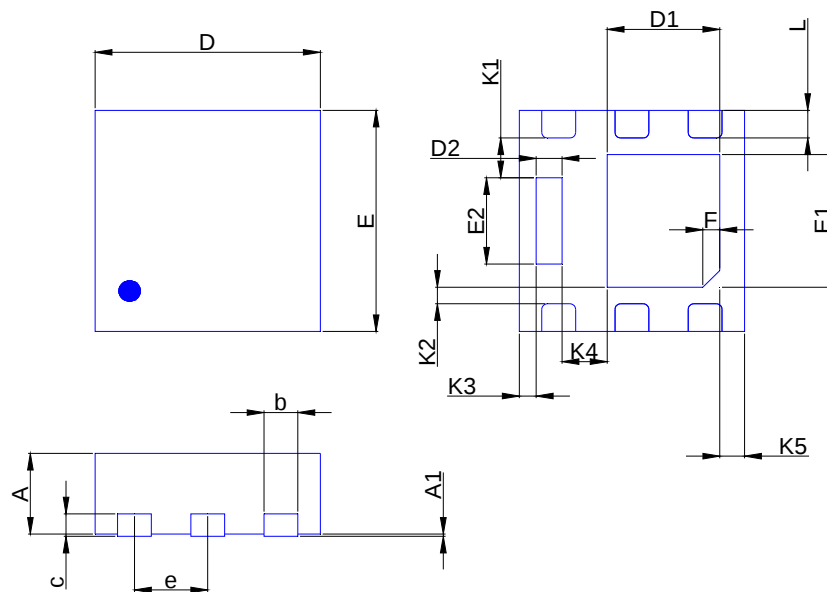
³Pulse width limited by maximum junction temperature.

Ordering & Marking Information:

Device Name: LB12N03A for EDFN 2 x 2



Outline Drawing



Dimension in mm

Dimension	A	A1	b	c	D	D1	D2	E	E1	E2	e	F	f	K1	K2	L	K3	K4	K5
Min.	0.50	0.00	0.25		1.9	1.0	0.13	1.9	1.1	0.65				0.306	0.10	0.2	0.10	0.27	0.17
Typ.		0.02	0.30	0.1	2.0	1.1	0.25	2.0	1.2	0.75	0.65	0.15	45°	0.356	0.15	0.25	0.15		0.22
Max.	0.65	0.05	0.35		2.1	1.2	0.35	2.1	1.3	0.88				0.406	0.20	0.3	0.20		0.27

Recommended minimum pads

